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(54) An error correction circuit

(57) An error correction circuit compensates for baseline wander which can occur when a data signal is passed through a DC isolation stage. The data signal, and its inverse are compared with a common reference level, and the error signal modifies the charge on a capacitor which forms part of a pair of negative feedback loop to control the baseline level.

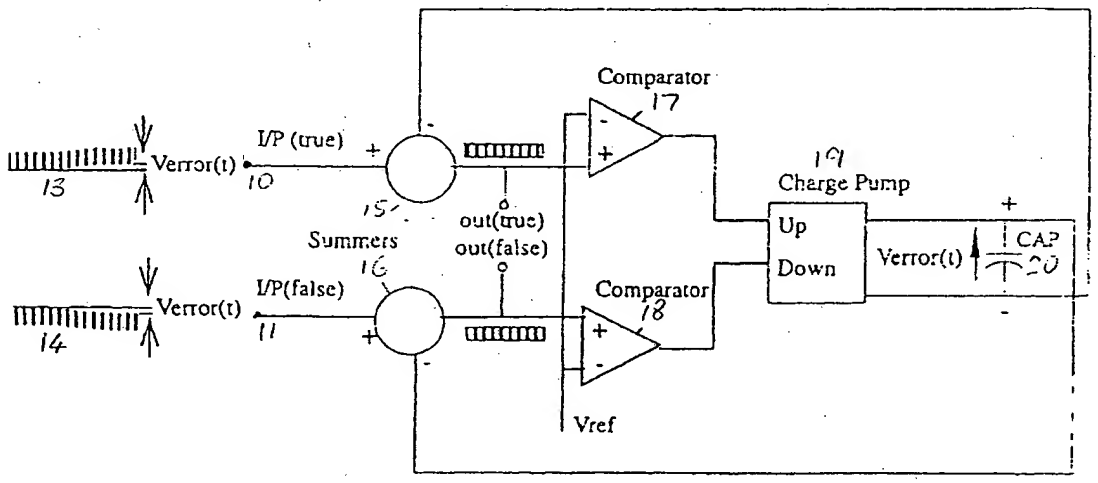

Fig 2

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Description

This invention relates to an error correction circuit, and is particularly concerned with data handling arrangements in which data is passed through an DC isolation stage. Such a stage preserves the AC signal component, but the data stream as a whole is free to drift, or float, relative to a particular potential reference, usually earth potential. If the mean potential of the data stream alters significantly, usually referred to as baseline wander, it may not be possible to decode accurately the data, and data errors may thereby be introduced into the data stream.

Circuits are known which have sought to correct for this particular difficulty, but such circuits have required carefully designed filters, and have been subject to instability resulting from the incorporation of positive feedback loops.

The present invention seeks to provide an improved error correction circuit.

According to this invention an error correction circuit includes a pair of comparators each of which is arranged to receive and compare a respective one of two complementary incoming data streams with a reference level, the outputs of the comparators being arranged to modify the potential across a capacitor, and the capacitor forming part of a pair of respective negative feedback loops, the feedback signal of a respective loop being combined with a respective one of the complementary incoming data streams so as to reduce baseline wander.

Preferably both comparators utilise the same reference potential.

Preferably again the output of both comparators is routed to a charge pump, which in turn has two output ports across which said capacitor is connected. Thus depending on the comparisons performed by the comparators, the potential across the capacitor will be modified, and furthermore the actual potentials on each terminal of the capacitor will change.

The invention is further described by way of example with reference to the accompanying drawings in which:

Figure 1 illustrates a known wander error correction circuit, and

Figure 2 illustrates an error correction circuit in accordance with the invention.

Referring to Figure 1, it will be seen that the known error correction circuit, requires the use of a pair of complementary filters 1,2, 3,4. The correct operation of this circuit demands positive feedback via the feedback loops 5, 6, and as a result the loop gain must be less than unity at all times, and if this condition is not satisfied, due to DC drift in the forward signal path, an irrevocable latch-up condition can result. The filters introduce cost and complexity, and can cause signal degradation.

Referring to Figure 2, the error correction circuit, which is in accordance with the present invention, has a pair of input ports 10, 11 to which digital data streams are applied. The stream applied to port 10 is the true data, whereas that stream applied to port 11 is its complement, ie inverse, and these two data streams typically are generated by a DC isolation transformer. Because of the DC isolation, the baseline can drift, or wander, and this effect is illustrated by the quantity Verror at the representations 13, 14 of the input data streams.

The data streams are passed via respective summers 15, 16 to an input of respective high gain comparators 17, 18, at which the data streams are compared with a common reference potential Vref. The results of the comparisons are applied to the Up-Down inputs of a charge pump 19, which is operative to modify the potential across the terminals of a floating capacitor 20. Thus the potentials on the two terminals of the capacitor are modified in dependence on the outputs of the comparators in response to the comparison of each data bit with the common reference Vref. The positive terminal of the capacitor 20 is connected as part of a negative feedback loop to the other input of summer 16, and the negative terminal of the capacitor 20 is connected as part of another negative feedback loop to the other input of summer 15. The true output data is obtained via terminal 21 connected to summer 15 and the false (complementary) output data is obtained via terminal 22 connected to summer 16.

Any voltage offsets and/or baseline wander on the incoming data, results in the threshold crossings in the comparators 17, 18. These threshold crossings are used to charge/discharge the capacitor 20 via the charge pump 19, and hence to produce an error voltage. As a consequence of high loop gain and negative feedback, the reconstructed error voltage is forced to track the DC and low frequency components of the data signal, and this is used to reduce or eliminate baseline wander.

Typically, the capacitor 20 has a value of 15pF, and the charge pump current is about 150μA. The circuit is intended for data rates of the order of 100 MHz and the maximum baseline frequency is approximately 20kHz.

As compared with Figure 1, the absence of in-line filters in Figure 2 implies that the error correction circuit is transparent to the data signal in the absence of baseline wander errors. Since the circuit utilises negative feedback, which has a high gain as the comparators have high gain, any DC drift in the forward signal is no longer critical.

Claims

1. An error correction circuit including a pair of comparators each of which is arranged to receive and compare a respective one of two complementary in-

coming data streams with a reference level, the outputs of the comparators being arranged to modify the potential across a capacitor, and the capacitor forming part of a pair of respective negative feedback loops, the feedback signal of a respective loop being combined with a respective one of the complementary incoming data streams so as to reduce baseline wander.

2. A circuit as claimed in Claim 1 and wherein both comparators utilise the same reference potential.

3. A circuit as claimed in Claim 1 or 2 and wherein the outputs of the two comparators are arranged respectively to control the up/down inputs of a charge pump, so as to control and modify the potential across said capacitor.

4. A circuit as claimed in any of the preceding claims and wherein said negative feedback loops each include a summer in the input path to a respective comparator, the summer thereby responding to variations of potential on said capacitor.

5. An error correction circuit substantially as illustrated in and described with reference to Figure 2 of the accompanying drawings.

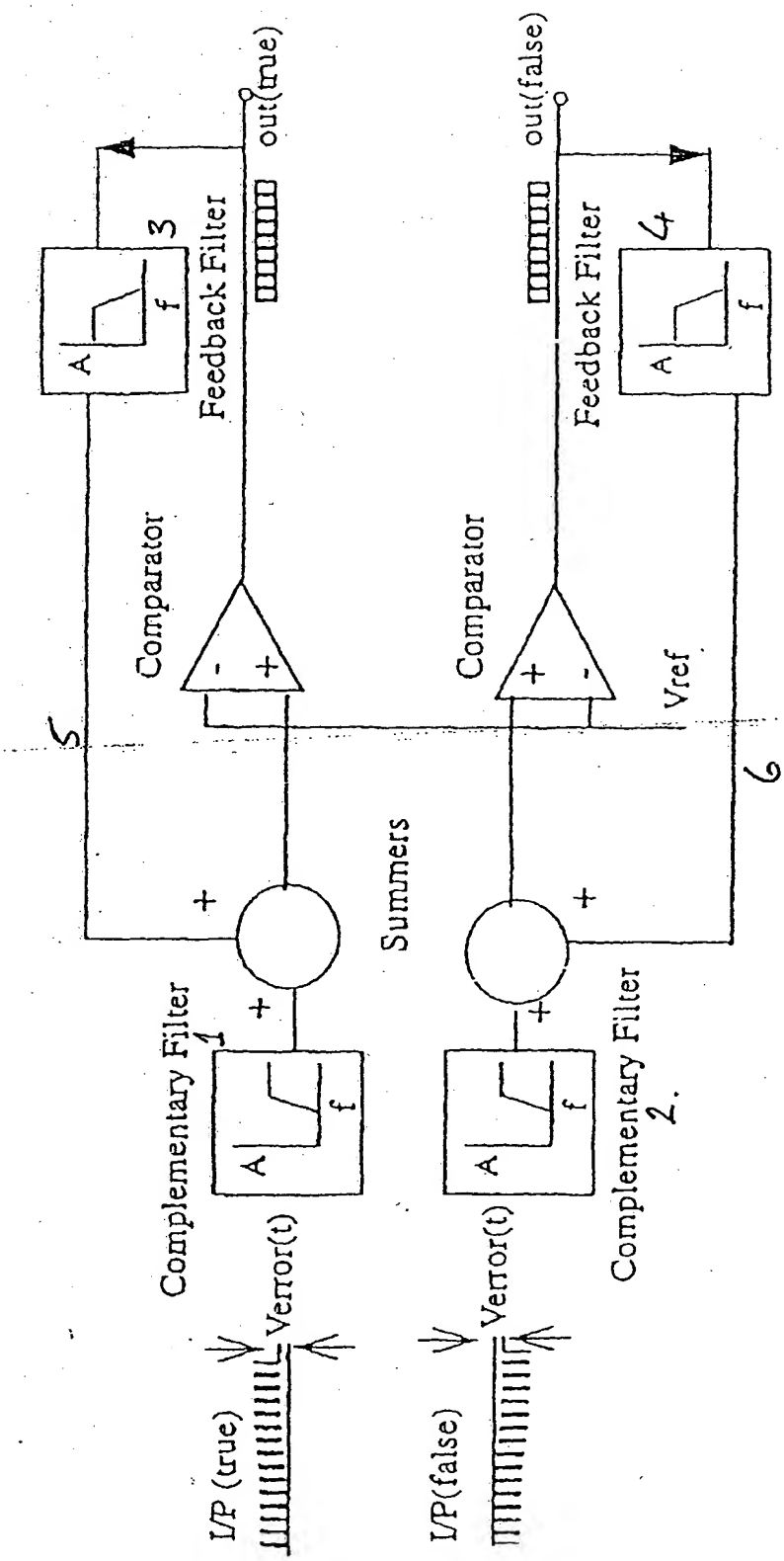

Fig 1

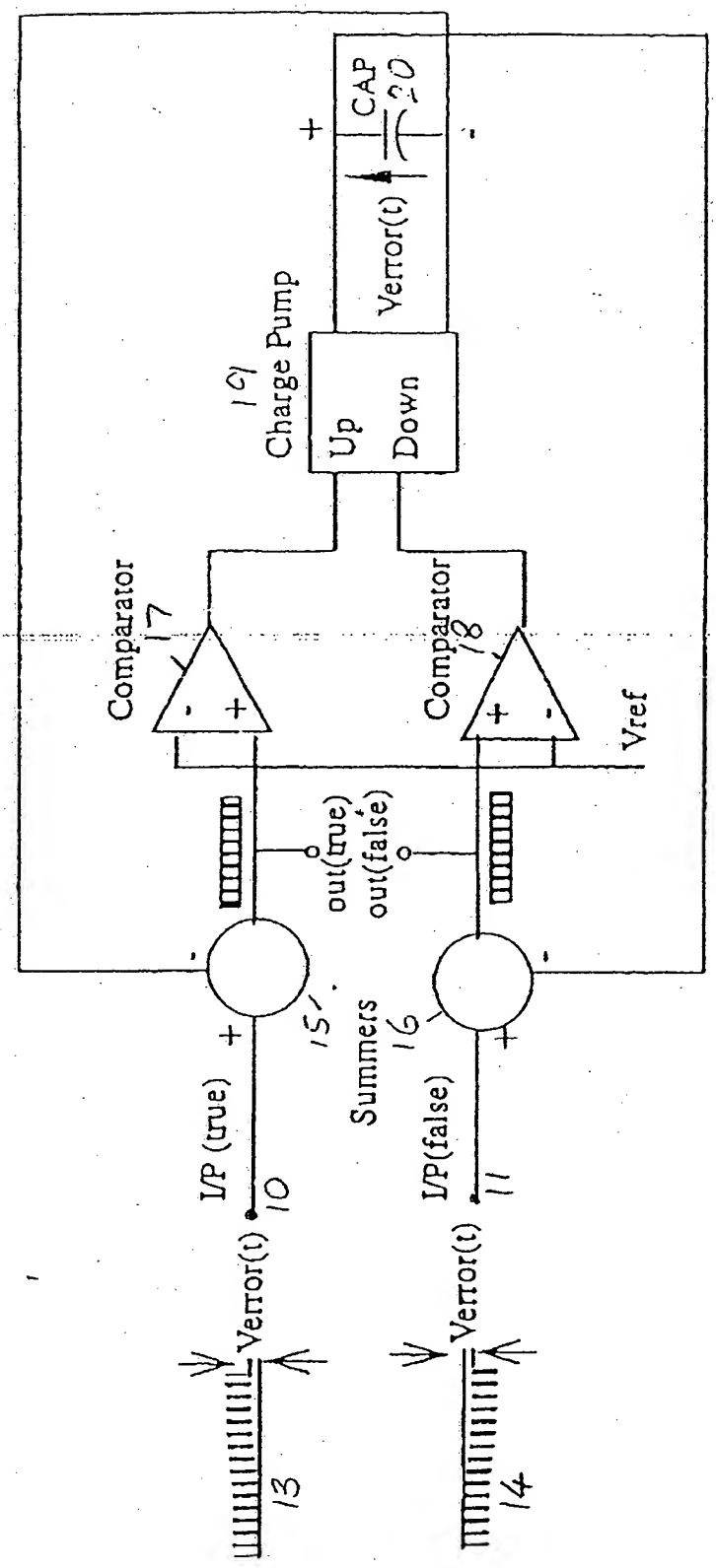

Fig 2

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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 1321

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	CN 1 077 830 A (BEIJING UNIV OF AERONAUTICS &) 27 October 1993 * abstract *	1	H03M13/00
A	GB 2 215 544 A (PLESSEY CO PLC) 20 September 1989 * page 2, line 3 - page 4, line 5; figures 3-5 *	1	
A	US 5 465 272 A (SMITH ROBERT W) 7 November 1995 * column 3, line 6 - column 3, line 44; figure 2A *	1	
A	EP 0 655 841 A (NOKIA MOBILE PHONES LTD) 31 May 1995 * column 5, line 11 - column 6, line 31; figure 2 *	1	
A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 013 (E-1304), 11 January 1993 & JP 04 243325 A (SANYO ELECTRIC CO LTD), 31 August 1992, * abstract *	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03M
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 391 (P-926), 30 August 1989 & JP 01 140016 A (YOKOGAWA ELECTRIC CORP), 1 June 1989, * abstract *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	25 April 1997	VILLAFUERTE ABR.., L

CATEGORY OF CITED DOCUMENTS

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